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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/613,776 | 07/02/2003 | Varadarajan Srinivasan | NLMI.P213 | 6968 |

25670 7590 04/06/2007

WILLIAM L. PARADICE, III
4880 STEVENS CREEK BOULEVARD
SUITE 201
SAN JOSE, CA 95129

| EXAMINER | |
|---|---|
| CHAN, SAI MING | |
| **ART UNIT** | **PAPER NUMBER** |
| 2609 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 04/06/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/613,776 | SRINIVASAN ET AL. | |
| | Examiner | Art Unit | |
| | Sai-Ming Chan | 2609 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

- Applicant's Amendment filed 3/26/2007 is acknowledged.
- Claims 6 and 10 have been amended
- Claims 13 to 16 are new

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 1-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Welin (U.S. Patent Application Publication # 2006/0007871 A1).**

Consider **claim 1**, Welin clearly shows and discloses a traffic management processor (page 42, claim 83 (single-chip integrated circuit) and abstract, lines 4-12) for scheduling packet (page 42, claim 83, lines 6-7 and paragraph 0017, lines 1-9, paragraph 0061, lines 1-5) for transmission across a network, comprising:

a departure time calculator (fig. 31, fig. 32, paragraph 0288, lines 1-3) for generating a departure time (page 42, claim 83, line 8 (deadline interval) and paragraph 0016, lines 1-6) for each packet; a departure time table having a plurality of rows, each having a first portion for storing the departure time (paragraph 0294, lines 1-5) for a corresponding packet and having a second portion for storing a rollover bit (fig. 32, paragraph 0018, lines 1-7 (S bit and MSB bit)); and a reset circuit (paragraph 0332, lines 1-9) coupled to the departure time calculator, the reset circuit configured to reset the rollover bits from a first logic state to a second logic state at a predetermined time (paragraph 0567, paragraph 0610, lines 5-7, paragraph 0632, lines 1-4, paragraph 0685, and fig.32)).

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 2, as applied to claim 1 above**, Welin clearly shows and discloses wherein the departure time calculator comprises: a counter for generating an arrival time (paragraph 0028, fig. 8, paragraph 0249, lines 6-7) ; and an arithmetic logic unit (paragraph 0677, lines 11-12 (ALU)) coupled to the counter and configured to generate the departure (paragraph 0287) in response to the arrival time.

Consider **claim 3, as applied to claim 2 above**, Welin clearly shows and discloses wherein the reset circuit has an output to provide a reset signal to the departure time table, wherein the reset signal is asserted to reset the rollover bits (paragraph 0018, lines 6-7 (S bit and MSB bit)) when the counter reaches a value indicative of the predetermined time (paragraph 0610, lines 5-6).

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the

time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 4, as applied to claim 1 above**, Welin clearly shows and discloses compare logic coupled to the departure time table and configured to compare the departure times with each other to determine which departure time is the earliest (paragraph 0685 and fig. 32).

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 5, as applied to claim 1 above**, Welin clearly shows and discloses wherein each rollover bit comprises a most significant bit (paragraph 0018, lines 6-7 (sign bit and MSB bit)) of the corresponding departure time.

Consider **claim 6,** Welin clearly shows and discloses a traffic management processor for scheduling packets for transmission across a network, comprising: a counter (paragraph 0249, lines 6-7) for generating an arrival time for each packet; an arithmetic logic unit (paragraph 0677, lines 11-12 (ALU)) having an input to receive the arrival time and configured to generate a departure time response to the arrival time; a reset circuit (paragraph 0332, lines 1-9) having an input to receive the arrival time and having an output for generating a reset signal; and a table having a plurality of rows, each having a first portion for storing the departure time (paragraph 0294, lines 1-5 )for a corresponding packet and having a second portion for storing a rollover bit, wherein the reset signal selectively resets the rollover bit from a first logic state to a second logic state (paragraph 0567, paragraph 0610, lines 5-7, paragraph 0632, lines 1-4, paragraph 0685, and fig.32)) .

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the

time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 7, as applied to claim 6 above**, Welin clearly shows and discloses wherein the reset circuit asserts the reset signal to reset the rollover bits (paragraph 0018, lines 6-7 (S bit and MSB bit)) when the counter generates a maximum arrival time (paragraph 0610, lines 5-6).

Consider **claim 8, as applied to claim 6 above**, Welin clearly shows and discloses wherein each rollover bit comprises a most significant bit (paragraph 0018, lines 6-7 (S bit and MSB bit)) of the corresponding departure time.

Consider **claim 9, as applied to claim 6 above**, Welin clearly shows and discloses compare logic (fig. 32 and paragraph 0685) coupled to the table and configured to compare the departure times with each other to determine which departure time is the earliest (paragraph 0685 and fig. 32).

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the

time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 10,** Welin clearly shows and discloses a method for operating a packet scheduler (page 41, claim 39, lines 1-10; page 42, claim 83, lines 6-7; and paragraph 0017, lines 1-9, paragraph 0061, lines 1-5), comprising: determining an arrival time for each of a plurality of packets received; calculating a departure time (claim 39, paragraph 0016, lines 1-6) for each packet in response to the packet's arrival time; storing the departure times for the plurality of packets in a departure time table; asserting a rollover corresponding to each departure time (paragraph 0018, lines 6-7 (sign bit and MSB bit)); and de-asserting the rollover bits when the arrival time reaches a maximum value (paragraph 0610, lines 5-6).

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 11, as applied to claim 10 above**, Welin clearly shows and discloses wherein the de-asserting comprises: comparing the arrival time with the maximum value (paragraph 0610, lines 5-6); and selectively asserting a reset signal in response to the comparing (page 36, paragraph 0688).

Consider **claim 12, as applied to claim 11 above**, Welin clearly shows and discloses resetting the rollover bits to a logic low value (page 36, paragraph 0688) in response to the reset signal.

Consider **claim 13, as applied to claim 10 above**, Welin clearly shows and discloses storing the rollover bits (fig. 32, paragraph 0018, lines 1-7 (S bit and MSB bit)) in the departure time table.

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 14, as applied to claim 13 above**, Welin clearly shows and

discloses the method, wherein each of a plurality of rows ' of the departure time table stores the departure time (paragraph 0294, lines 1-5) and the rollover bit (fig. 32, paragraph 0018, lines 1-7 (S bit and MSB bit)) for a corresponding packet.

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 15, as applied to claim 11 above**, Welin clearly shows and discloses the method, wherein the reset signal is asserted by a reset circuit (paragraph 0332, lines 1-9) that is coupled to the departure time table.

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

Consider **claim 16, as applied to claim 15 above**, Welin clearly shows and discloses the method, wherein the departure time ((paragraph 0294, lines 1-5)) is calculated by a departure time calculator ((fig. 31, fig. 32, paragraph 0288, lines 1-3)) that is coupled to the departure time table and to the reset circuit.

Although Welin does not explicitly show a table with plurality of rows of departure time, the reference does identify a single departure time and rollover (msb) bit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

***Response to Arguments***

Applicant's arguments, see page 7, lines 30-31, page 8, lines 1-2, lines 29-30, page 9, lines 1-9, lines 25-30, and page 10, lines 1-2, filed 3/26/2007, with respect to the rejection(s) of claim(s) 1-12 under U.S.C 102 (e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of U.S.C. 103 (a) violations. The applicant stated in the remark that Welin does not show a table with a plurality of

row with each row containing a departure time and rollover bit. Welin does disclose and show departure time and rollover bit. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Welin's identification of a single departure time and rollover (MSB) bit to construct a table with plurality of rows, with each row containing a departure time and rollover bit, so that the packets will depart in an orderly fashion.

## *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication : US 2003/0016686 A1, inventer: Wynne et al., issued: 1/23/2003.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**Hand-delivered responses** should be brought to

Customer Service Window
Randolph Building

401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Sai-Ming Chan whose telephone number is (571) 270-1769. The Examiner can normally be reached on Monday-Thursday from 6:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rafael Pérez-Gutiérrez can be reached on (571) 272-7915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

***Sai-Ming Chan***

S.C./ sc

March 30, 2007

RAFAEL PEREZ-GUTIERREZ
SUPERVISORY PATENT EXAMINER

3/30/07